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Efficient Current Mode Sense Amplifier for Low Power SRAM

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Abstract

Sense amplifiers are one of the most vital circuits in the margin of CMOS memories. Their performance influences both memory access time and overall memory power dissipation. The existing Current-Mode Sense Amplifier coupled with a simplified read-cycle-only memory system has the ability to quickly amplify a small differential signal on the Bit-Lines (BLs) and Data-Lines (DLs) to the full CMOS logic level without requiring a large input voltage swing. The Current-Mode Sense Amplifier has two levels of sensing schemes. This hierarchical two-level sensing scheme helps in reducing both power consumption and sensing delay imposed by the bit-lines and the data-lines on high density SRAM designs. This type of Current-Mode Sense Amplifier improves the sensing speed and reliability of the previously published designs and at the same time reduces the power consumption to a considerable extent. In order to further improve the performance of the existing current-mode sense amplifier, an efficient current-mode sense amplifier is proposed in this research. The proposed research work uses the clamped bit-line sense amplifier.

Keywords: *Current mode and sense amplifier, low power, low voltage SRAM.*

1. Introduction

SRAM cells are known to be highly sensitive to process variations due to the extremely small device sizes. Due to the high demands on the portable products, power consumption is a major concern in VLSI chip designs [1]. Especially, the low power static random access memory (SRAM) becomes more important because the number of memory cells and the bit width continue to be larger. With technology scaling, the requirements of higher density and lower power embedded SRAMs are increasing exponentially. It is expected that more than 90% of the die area in future system-on-chip (SoC) will be occupied by SRAM [14]. This is driven by the high demand for low-power mobile systems; RAM is an important part of modern microprocessor design, taking a large portion of the total chip area and power. Increasing the density of SRAM caches provides an effective method to enhance system performance. Scaling device size doubled the transistor count every two years according to Moore's law, and hence the density of SRAM caches kept mounting every next generation [13].

SRAM represents a large portion of the chip, and it is expected to increase in the future in both portable devices and high-performance processors. To achieve longer battery life and higher reliability for portable application, low-power SRAM array is a necessity [4]. Several techniques have been proposed to reduce the power consumption of SRAMs. As on-chip memory will occupy a large portion of the chip area; the power dissipated within the memory, both active and standby will become a dominant part of the total power consumption of the chip[2], [4]. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represents the active power consumption.

Sense amplifier is one of the important peripheral circuits in the memory as it strongly influences the memory access times [9]. It retrieves the stored data from the memory array by amplifying the small differential signal on the bit-lines. One of the key challenges that limit the performance of sense amplifiers is the increasing bit-line capacitances [8], [12]. In advanced memories the capacitances of the bit-line is increasing due to technology scaling and the increasing number of cells attached to the column. In such memories voltage mode cannot keep up to their performance thereby leading to the need for faster sensing techniques that are not affected by the bit-line capacitance [13]. Current mode sense amplifier are applied to reduce the sense circuit delays as they provide low common input/output impedances and they have the ability to quickly amplify a small differential signal on the bit-lines (BLs) and data-lines (DLs) to the full CMOS logic level without requiring a large input voltage swing, is widely used as one of the most effective ways to reduce both sensing delay and power consumption of the SRAM. The small input impendence presented to the bit-lines result in reduced voltage swings, cross-talk and substrate currents. The current mode

sense amplifier converts and amplifies a small current difference into CMOS voltage levels. The following sections describe different type of current mode sense amplifier and due to its inherent advantage of performance over voltage mode sense amplifier.

This paper presents a current-mode SA that improves the sensing speed and reliability of the previously published designs and at the same time reduces the power consumption. It was extensively simulated and graphically presented in comparison with other widely used SA topologies, namely the high-speed [11], decoupled latch [5], [6], the alpha latch [7] designs and read only memory system [1] designs.

Paper Organization

The rest of the paper is organized as follows. In Section 2 Existing systems. Section 3 Result. Finally, we draw our conclusions in Section 4.

2. Existing Designs

Current mode sense amplifier is used to detect the current difference between the bit lines to determine whether a '1' or '0' is stored in the memory cell. It directly measures the cell read current and transfers it to the output circuits. This approach can overcome the restriction of gain reduction brought on by voltage mode sense amplifier at low power supply voltage [13]. This section briefly describes the operations of existing designs studied in this work. In this current conveyer sense amplifier will be used as the benchmark to evaluate the performance of other current mode sense amplifiers.

2.1 Current Conveyor-Based Sense Amplifier

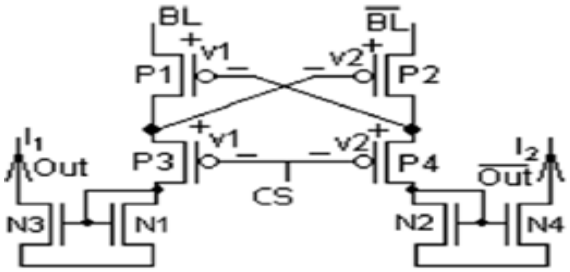
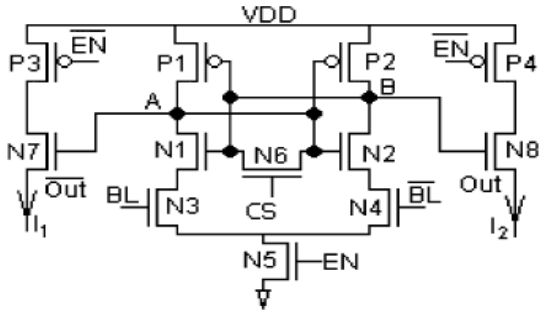


Fig. 1. Current Conveyor

The conveyor-based sense amplifier was consists of four identical pMOS transistors [P1–P4 in Fig.1] connected in a feedback structure. It is assumed that the complementary bit-lines (BL and BL') are pre-charged to V_{DD} and all four pMOS transistors operate in saturation region during the read cycles. The current conveyor is enabled by triggering the column select (CS) signal low. Since all four transistors are in saturation, their source-to-drain currents are only dependent on their gate-to-source voltages. As a result, voltage at the bit-line terminals (VBL and VBL') is the same and equal to (V1 + V2). The current conveyor therefore has the ability to convey the differential current from the bit-lines to the data-line without waiting for the discharging of the highly capacitive bit-lines [8].

Thus, this design achieved both higher sensing speed and lower power consumption when compared to the conventional voltage mode designs in which large voltage difference must be developed between the bit-lines [8]. Based on this basis structure, several improved versions of this design have been reported, mainly by adding current mirrors to the feet of the current-conveyor to enhance its current drivability [9], [10], [11]. This paper compares new current mode sense amplifier with the high-speed design [11] which consists of four additional nMOS transistors shown in Fig. 1. These nMOS devices form two current-mirrors to intensify the output currents I1 and I2 to the data-lines. This design will be used as the benchmark to evaluate the performance of other current mode sense amplifiers.



2.2 Alpha-Latch Sense Amplifier

Fig. 2. Alpha Latch

The alpha latch [7] is depicted in Fig. 2. The nMOS transistor N5 is used to turn the amplifier off during standby thus saves power. When the sense amplifier is activated by the enable signal (EN), the differential input from the complementary bit-lines induces a differential trans-conductance in N3 and N4. As a result, voltage and current differences will appear at the drains of N3 and N4, i.e., the sources of N1 and N2. Since the CS signal turns off N6, the flip-flop structure will latch and full swing voltages will be available at nodes A and B, turning one of the transistors N7 and N8 on while the other is off. During standby, EN' is kept high to turn P3 and P4 off. During operation, both P3 and P4 are turned on but one of N7 and N8 is turned off, thus only one current will flow to the data-lines to the output of SRAM.

2.3 Decoupled Latch Sense Amplifier

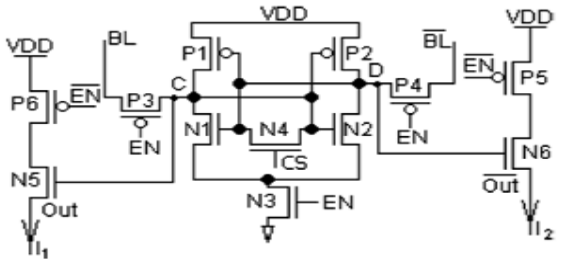


Fig. 3. Bit-line decoupled latch

The decoupled-latch consists of six nMOS and two pMOS transistors, as shown in Fig. 3. Similar to the alpha-latch, its N3 is used to save power. The reason of use a tail nMOS device in Fig.2 and Fig.3 is because it gives a smaller area comparing to a pMOS with the same current strength. Furthermore, BLs. is pre-charged to V_{DD} and hence nMOS tail device is required.

It is in contrast with read cycle only memory systems design in Fig. 4 where a tail pMOS device must be used because DL and DL bar are pre-charged to ground. To tackle the heavily loaded bit-lines issue, these bit-line signals are tapped to the input ports of the amplifier through two decoupled devices, i.e., P3 and P4. Once the bit-line differential signal is induced at nodes C and D, the latch is enabled by turning off N4 but turning on N3. Concurrently, P3 and P4 are turned off to decouple the bit-lines from the high-swing output nodes. The use of P3 and P4 helps reducing the impact of the bit-line capacitances on the switching activity, hence significantly reducing both sensing delay and power consumption[5], [6]. Similar to the alpha latch design, full swing voltage at nodes C and D is transferred to the data-line differential voltage by the means of a pair of nMOS transistors, as shown in Fig. 3.

2.4 Read Cycle Only Sense Amplifier

This Sense Amplifier is coupled with a simplified read-cycle-only memory system [14], is presented in Fig**.** 4. It consists of two sensing stages: local and global. The local sensing stage is formed by four pMOS (P3–P6) and three nMOS (N1, N2, and N7) transistors. While P3 and P4 act as a column switch, the rest of the transistors establish the local cross-coupled inverters, which are responsible for generating the BL differential currents and transferring them to the DLs. The global sensing stage consists of three pMOS (P7–P9) and five nMOS (N3–N6 and N8) transistors. In Fig. 4, two output inverters, which serve as buffers to drive the potentially large output loads to full CMOS logic output levels, are also included. The operation of the proposed Sense Amplifier is described as follows.

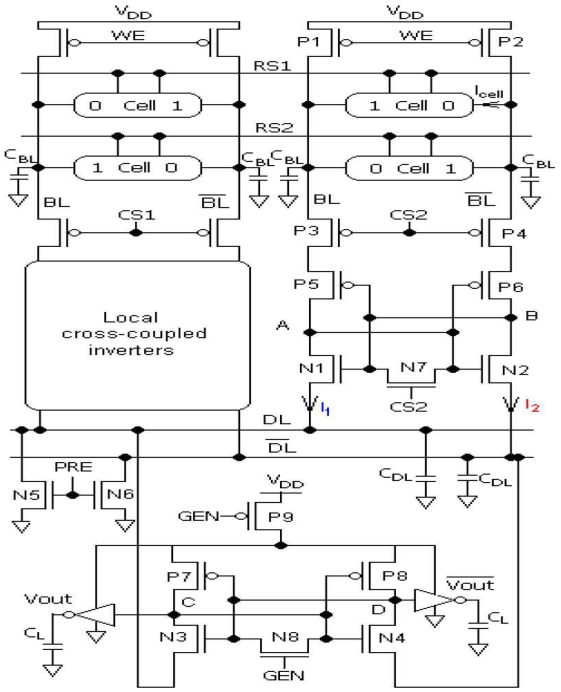


Fig. 4. Proposed design coupled with a simplified read-cycle-only memory system

During the standby period, P3 and P4 are turned off to block any BL currents. The Column Select and Global Enable (CS and GEN) signals turn on N7 and N8 respectively to equalize nodes A, B and C, D to the same potential, respectively. Meanwhile, two pre-charge transistors N5 and N6 are turned on to pull both DLs to ground. At the same time, P9 is turned off to save power. Since P9 is off and the DLs are pre-charged to ground, C and D are also at a low potential (near V_{th}) during standby. The two output inverters are also cut-off by P9, as shown in Fig. 4. This topology ensures that the standby current of the circuit, and thus the power dissipation are minimized.

Consider both RS1 and CS2 being activated during a read operation. The pre-charge signal (PRE) turns N5 and N6 off, allowing the DL voltages to change freely. The memory cell at the upper row and right column will be selected, resulting in a small cell current I_{cell} flowing from BL bar the into the cell as shown in Fig.4 and discharges the BL bar to a voltage level lower than that of the BL. As CS2 is triggered low, P3 and P4 are turned on to transfer the BL potentials and BL currents to the inputs of the local cross-coupled inverters. At the same time, N7 is turned off to activate the local cross-coupled inverters. This building block senses the voltage and current difference at the source terminals of P5 and P6 and quickly finishes its latching process. Hence, node A is pulled to V_{DD} while node B is discharged to the same potential of the DL bar, which is near ground, More importantly, during this latching process, the pulsing current flowing from N2 to DL bar, i.e., is much higher than that from the N1 to the DL. This phenomenon can be intuitively explained as follows.

During standby, nodes A and B reside at a low potential near V_{th}. Once the sense amplifier is activated, both node potentials will slightly rise and then quickly start to deviate. For example, node A approaches near V_{DD} while node B plunges to near ground. Thus, transistor N1 is in cutoff most of the time. On the other hand, transistor N2 operates in triode region and then moves to saturation region, resulting. In a much larger pulsing current when compared to that of N1. Integrating these two currents over time we get the total charges flowing to DL and DL bar, respectively.

These differential currents flow to the DLs and induce a voltage difference on the global data-lines. Similarly, this voltage difference is amplified by the global sensing stage to the intermediate outputs V_C and V_D, also shown in Fig. 4. These two voltages are then fed to the output buffers to get the full CMOS logic levels. It is worth mentioning that the global sensing stage can only be activated after the latching process of the local amplifier has completed. This hierarchical two-level sensing scheme helps reducing both power consumption and sensing delay imposed by the bit-lines and the data-lines on high density SRAM designs. The global sensing stage is required to amplify the small differential signal on the data-lines to a full CMOS logic level at the output of the SRAM.

The total active power dissipated in the proposed SA is limited by the cell current flowing from one of the BLs to the node of the cell where a "0" is stored (which solely depends on the cell design) and the switching currents of the sensing stages. After latching, the cross-coupled configuration stays at one of its bi-stable stages and no additional current is consumed and hence, power dissipated on the BLs and DLs is optimized. Sensing delay is defined from the time when CS signal reaches half V_{DD} to the time when the differential output reaches half- V_{DD}. Since the global data-lines are shared among many columns, their parasitic capacitances are significant and have an important impact on the input margin of the global sensing stage. The voltage difference on the data-lines must be larger than the input offset voltage of the global sense amplifier in order to perform a correct readout. Thus, number of columns sharing the data-lines should be considered carefully to maintain a reasonable input margin. It is determined by the size of the MOS transistors in the local sense amplifier (i.e., N1–N2 and P5–P6).

In the design of the memory cell, for obtaining the better results like less power dissipation minimum delay sense amplifiers are used. Different types of sense amplifiers are used in memory design according to their performance. The delay of the sense amplifier should be very small so that it can detect even the small change on the bit lines as the read and write operation get starts. Sense amplifier reduces the power dissipation of the whole circuit. While design the sense amplifier, it is kept in mind that the delay and power dissipation remain minimum.

2.5 Proposed Work

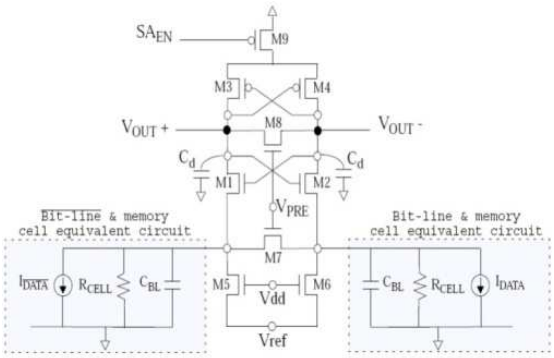


Fig. 5. Clamped Bit Line Sense Amplier

The power dissipation and delay of the sense amplifier circuit can be further reduced by using Clamped Bit Line Sense Amplifier (CBLSA), shown in fig. 5. Using this amplifier, the voltage on the bit-line is clamped to a stable voltage (V_{REF}) the signal current produced by the cell can transferred to an internal sense amplifying node without charging/discharging the large bit-line capacitance. So that both the sensing delay and power is further reduced and it is used in low power application.

This sense amplifier uses three pre-charge and equalization transistors (M7, M8 and M9), two current sensing transistors (M5 and M6) and four back to back inverter configuration transistors for the voltage output stage (M1, M2, M3, M4). Its operation follows two stages pre-charge/equalization, and sensing. The following is the timing schedule 1) transistors M7, M8, M9 are turned on to pre-charge and equalize the sensing nodes, 2) transistors M7 and M8 are turned off and the memory cell will be accessed, 3) the current from the cell is started being sourced by one of the transistors M1 and M2, 4) then a voltage difference is started forming on one of the output nodes, 5) Finally, this voltage is further amplified by the positive feedback amplifier until it reaches the latched state.

Another observation is that this amplifier maintained a constant speed over increased bit-line capacitance. To recognize the power savings of current sensing amplifiers there is a need to examine the dynamic power dissipation of the voltage sensing amplifier. In voltage sensing, the bit-line are discharged and charged by dV_{BL} (close to 400mV) for every read operation. When this dV_{BL} is combined with both increasingly large bit-line capacitance CBL, and read frequency "f_{read}" the energy following the below equation becomes large.

$$P = C_{BL} \cdot V_{BL}^2 \cdot f_{read}$$

The current sensing amplifier on the other hand has a very negligible voltage swing, thus nearly eliminating dynamic

power dissipation. Furthermore, this bit-line voltage inactivity significantly decreases cross talk between bit-lines, and supply voltage drop associated with bit-line charge up.

3. Results

This chapter deals with simulation results of the Current mode sense amplifiers. The simulation tool used is TANNER. The power analysis is obtained with the help of TANNER tool. The simulation results are shown as follows.

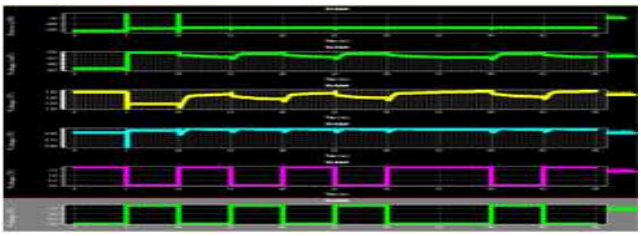


Fig. 6. Waveform of current conveyer based sense amplier

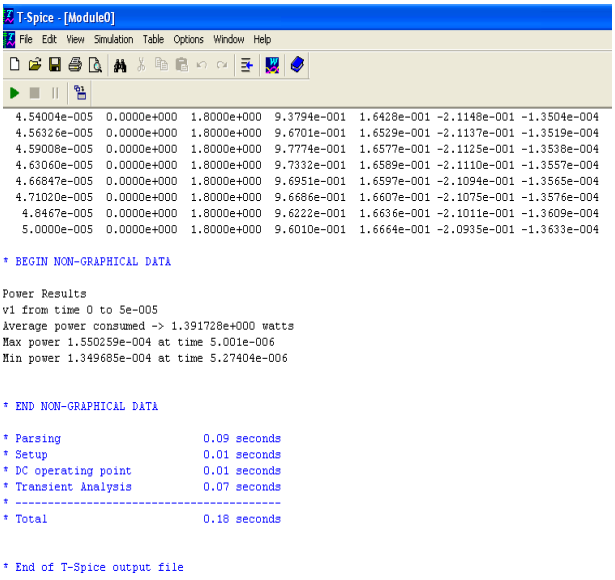


Fig. 7. Power analyasis of current conveyer based sense amplier

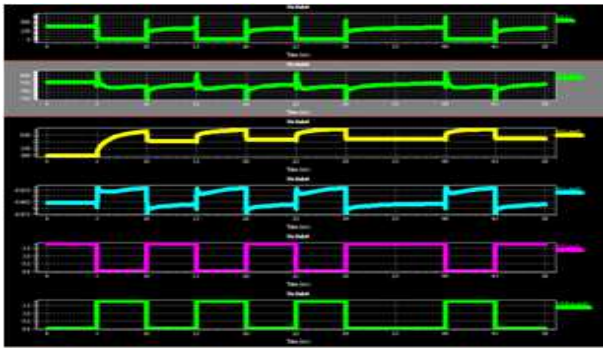


Fig. 8. Waveform for alpha latch sense amplifier

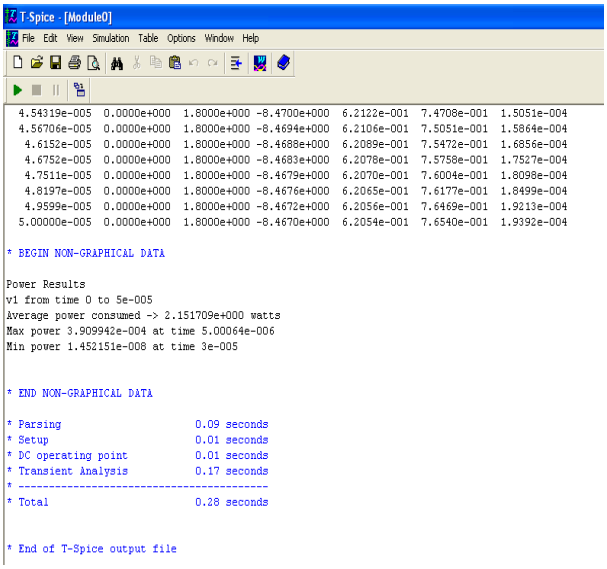


Fig. 9. Power analysis of alpha latch

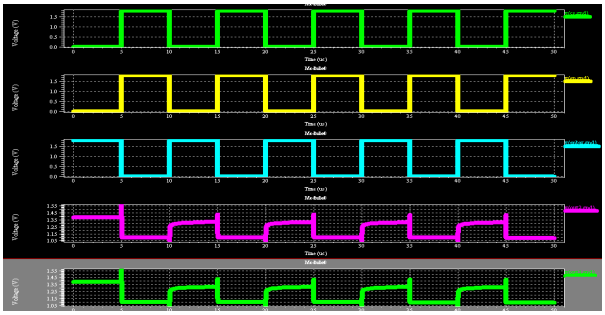


Fig. 10. Waveform for bit line decoupled latch sense amplifier

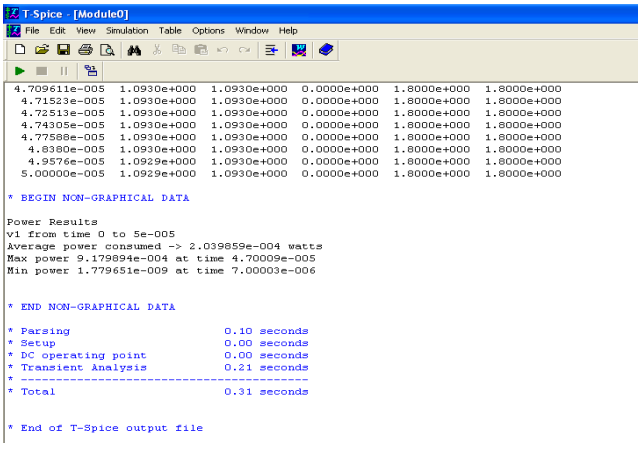


Fig. 11. Power analysis of bit line decoupled latch sense amplifier

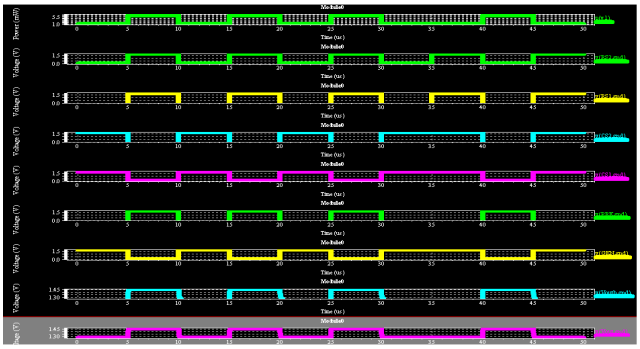


Fig. 12. Waveform for Read cycle only memory system

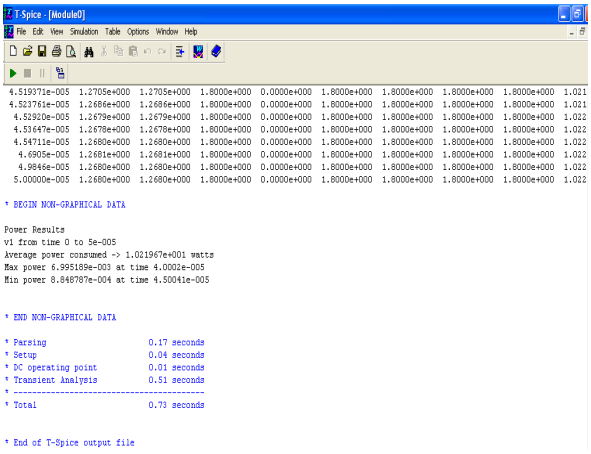


Fig. 13. Power analysis of read cycle only memory system

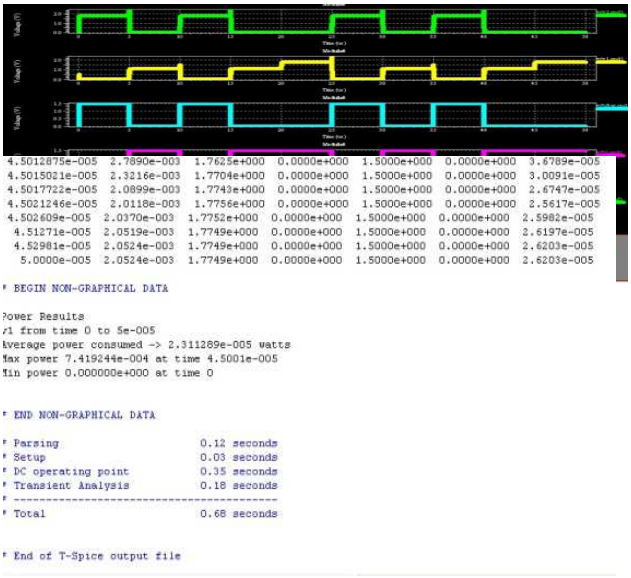


Fig. 14. Clamped Bit Line Current Sense Amplifier

Fig. 15. Power analysis Clamped Bit Line Current Sense Amplifier

4. Conclusion

Sense amplifiers are one of the most vital circuits in the margin of CMOS memories. Their performance influences both memory access time and overall memory power dissipation. The Current-Mode Sense Amplifier coupled with a simplified read-cycle-only memory system, has the ability to quickly amplify a small differential signal on the Bit-Lines (BLs) and Data-Lines (DLs) to the full CMOS logic level without requiring a large input voltage swing. This current-mode Sense Amplifier having two levels of sensing scheme, helps reducing both power consumption and sensing delay imposed by the bit-lines and the data-lines on high density SRAM designs. This improves the sensing speed and reliability of the previously published designs and at the same time reduces the power consumption to a considerable extent. Thus it can be concluded that the existing SA is best suited for applications where low-voltage, low-power, high-speed and stability are of crucial design considerations. This paper mainly focuses on reducing the power dissipation and delay of the sense amplifier circuit by using Clamped Bit Line Sense Amplifier (CBLSA).

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